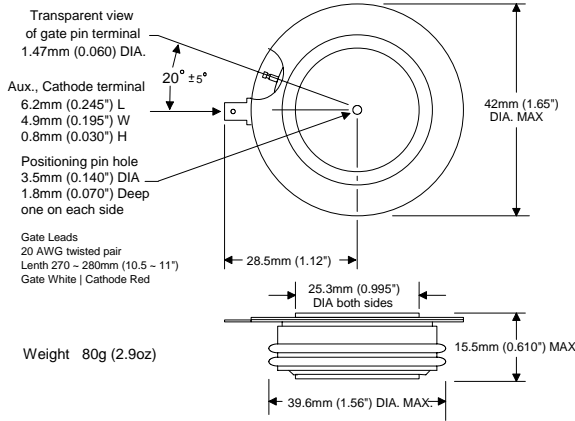


E package

JEDEC: TO-200AA



Part number scheme

E T 07 N 18 KNX
 1 2 3 4 5 6

- 1) Package designation
- 2) Thyristor designation (i.e. SCR)
- 3) Series number
- 4) Designates standard recovery time
- 5) Voltage Multiplier (example: 18 x 100 = 1800)
- 6) Proprietary suffix

Features:

- ✓ All diffused silicone.
- ✓ Center amplifying gate.
- ✓ Standard recovery time for phase control applications.
- ✓ Disk press package (nick named, Hockey Puck)
- ✓ Metal and ceramic package construction.
- ✓ Double side cooling.

Voltage

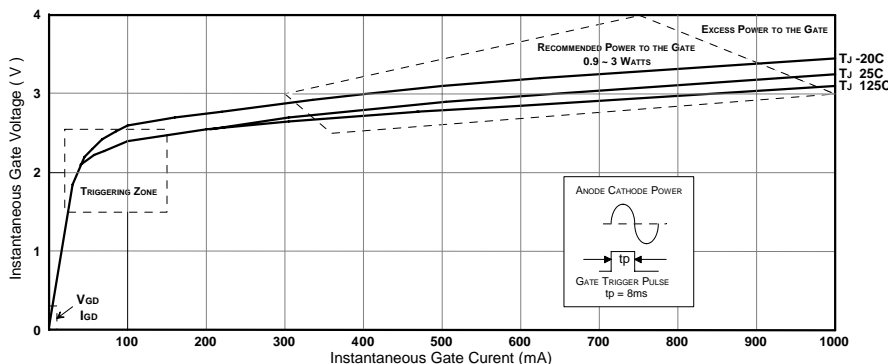
Parameter	Symbol	Rating	Units
Maximum Repetitive Off-State Voltage <small>Notes: 1, 3, 4, 5, 6, 7</small>	V_{DRM}	1600 ~ 2600	Volts
Maximum Repetitive Reverse Voltage <small>Notes: 1, 3, 4, 5, 6</small>	V_{RRM}	1600 ~ 2700	Volts
Maximum non repetitive Surge of Reverse Voltage <small>Notes: 2, 3, 4, 5, 6</small>	V_{RSM}	$V_{RRM} + 100$	Volts
Critical rate of rising off-state Voltage, Linear to 80% of V_{DRM} <small>Note: 2</small>	dv/dt	200	V/ μ s
<small>Note 1: T_J 25°C. Note 2: T_J 125°C. Note 3: Measured at the peak of the sine wave, Note 4: Below 0°C derate V_{DRM} and V_{RRM} 10%. Note 5: V_{DRM} and V_{RRM} have I_{DRM}, I_{RRM} of up to 35mA. Note 6: V_{DR} and V_{RR} have typical I_{DR}, I_{RR} of 2~7mA. Note 7: For DC applications derate V_{DRM} 45%.</small>			
Specifying voltage:	1800V, ET07N18 1600V, ET07N16	2200V, ET07N22 2000V, ET07N20	2600V, ET07N26 2400V, ET07N24 Above 2600V inquire for availability.

Gate

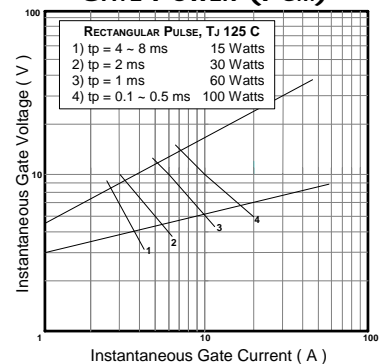
Parameter	Symbol	Rating			Units
		Temp.	Typ.	Max.	
Gate Trigger Voltage <small>Note 3</small>	V_{GT}	-20°C 25°C 125°C	2.7 ~ 3.5 2.6 ~ 3.3 2.5 ~ 3.1	3.5	Volts
Maximum Gate Trigger Current <small>Notes 1, 3</small>	I_{GT}		300		mA
Minimum Forward Current to Latch on-state <small>Notes 1, 5</small>	I_L		800		mA
Maximum permissible Gate Voltage not to Trigger <small>Notes 1, 3</small>	V_{GDM}		250		mV
Maximum permissible Gate Current not to Trigger <small>Notes 1, 3</small>	I_{GDM}		10		mA
Maximum peak non repetitive Gate Voltage <small>Notes 2, 3</small>	V_{GM}		8.4		Volts
Maximum Negative Gate Voltage <small>Notes 2, 4</small>	$-V_{GM}$		5		Volts
Maximum non repetitive Gate Current <small>Notes 2, 3</small>	I_{GM}		3.7		Amperes
Maximum Repetitive Gate Current <small>Notes 2, 3</small>	I_{GRM}		1		Amperes
Average Gate Power (recommended) <small>Note 2, 3</small>	$P_{G(AVE)}$		0.9 ~ 3		Watts
<small>Note 1: T_J 25°C. Note 2: T_J 125°C. Note 3: Rectangular pulse, $t_p \leq 8.3$ ms. Note 4: Rectangular $-V_{DC}$ pulse, $t_p \leq 8.3$ ms. Note 5: Test conditions: I_{DC} $R_L = 12\Omega$.</small>					

These graphs depict a typical device, each device has unique characteristics

Gate Characteristics



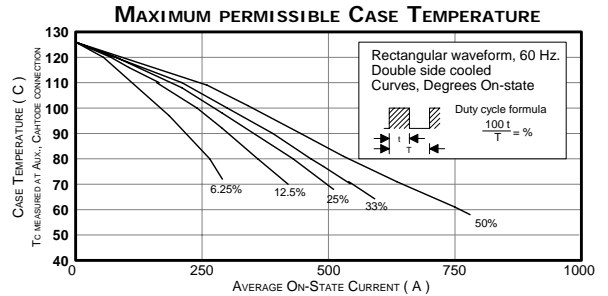
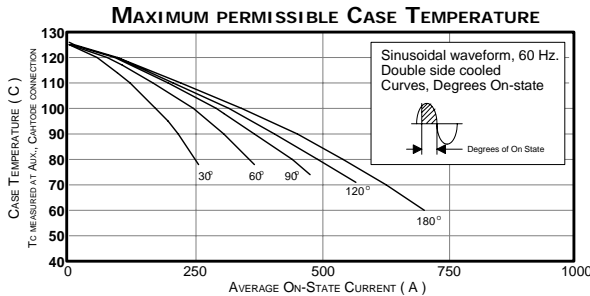
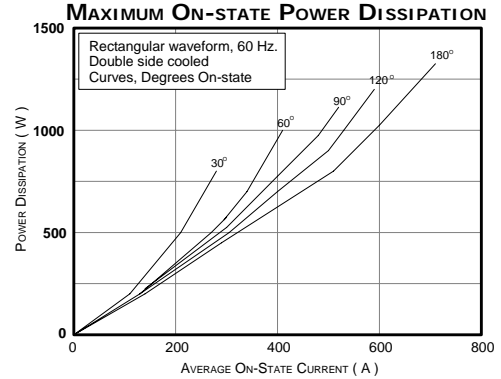
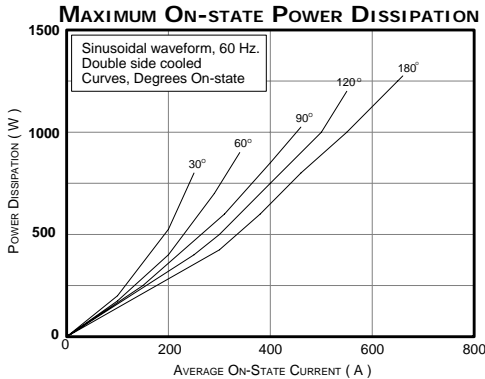
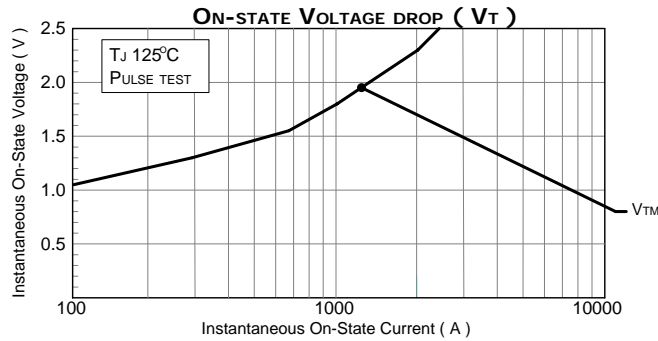
Maximum non repetitive GATE POWER (PGM)



Amperage

Parameter	Symbol	Rating	Units
Maximum, Average, On state, Current <small>Notes: 3, 4</small>	$I_{T(AVE)}$	700	Amperes
Maximum, RMS, On state, Current <small>Notes: 3, 5</small>	$I_{T(RMS)}$	1000	Amperes
Maximum non repetitive, Surge, On state, Current, with no reverse voltage reapplied. <small>Notes: 2, 4</small>	$I_{TSM} 0\%V_{RRM}$	8	kA
Maximum non repetitive, Surge, On state, Current, with maximum reverse voltage reapplied. <small>Notes: 2, 4</small>	$I_{TSM} 100\%V_{RRM}$	7	kA
Critical rate of rising On-state Current, non repetitive <small>Note: 6, 7</small>	di/dt	400	A/ μ s
Holding Current <small>Notes: 1, 5</small>	I_H	400	mA
I_{DR} = Repetitive, Off-State, leakage Current (typical) <small>Note: 1</small> I_{RR} = Repetitive, Reverse, leakage Current. (typical) <small>Note: 1</small>	I_{DR} & I_{RR}	2 ~ 7	mA
I_{DRM} = Maximum (threshold), Repetitive, Off-State, Current. <small>Note: 1</small> I_{RRM} = Maximum (threshold), Repetitive, Reverse, Current. <small>Note: 1</small>	I_{DRM} & I_{RRM}	35	mA
Fuse's absolute maximum $I^2 t$ with no reverse voltage reapplied <small>Note: 2, 4</small>	$I^2 t, 0\% V_{RR}$	265	kA
Fuse's absolute maximum $I^2 t$ with up to 80% of V_{RRM} reapplied <small>Note: 2, 4</small>	$I^2 t, \leq 80\% V_{RRM}$	187	kA
Reverse Recovery Charge (C_S = Stored Charge)	Q_{RR}	Consult factory	μ Cs
<small>Note 1: T_J 25°C. Note 2: T_J 125°C. Note 3: T_{Case} 55°C, double side air cooled. Note 4: 180° conduction, 60Hz sine wave. Note 5: Test conditions: I_{DC} $R_L = 12\Omega$. Note 6: Switching from $V_{DRM} \leq 1000V$ Note 7: In addition to 0.2μF and 20Ω snubber circuit</small>			

These graphs depict a typical device, each device has unique characteristics



Thermal & Mechanical

Parameter	Symbol	Rating	Units
Operating Temperature Range	T_J	-40° ~ 125°	°Celsius
Maximum Thermal resistance, Junction to Case <small>Notes:1, 3, 5</small>	R_{th-J-C}	0.06	°C/W
Maximum Thermal resistance, Case to Heat Sink <small>Notes: 1, 2, 3, 4, 5</small>	$R_{th-C-hs}$	0.03	°C/W
Mounting Pressure		450 ~ 1100	kg
		1000 ~ 2500	lb.
<small>Note 1: Recommended mounting pressure applied Note 2: Mounting surfaces flat and greased Note 3: Double side cooled Note 4: Case Temperature measured at aux., cathode Note 5: 180° on-state</small>			