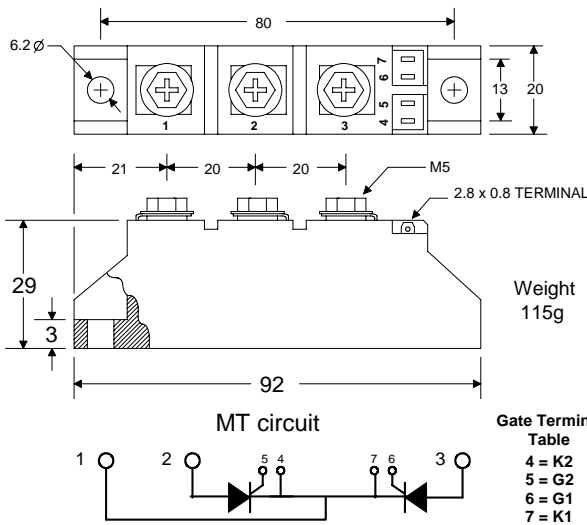


## TO-240AA compatible package



Part number scheme

**PS MT 25 N 16 STD**  
 1 2 3 4 5 6

- 1) Power Semiconductors initials
- 2) Circuit designation
- 3) Series number
- 4) Designates standard recovery time
- 5) Voltage Multiplier (example: 16 x 100 = 1600 Volts)
- 6) Proprietary suffix

## Features:

- ✓ All diffused silicone junctions.
- ✓ Standard recovery time for phase control applications.
- ✓ Module package compatible with JEDEC TO-240AA.
- ✓ Thick copper base plate.
- ✓ Isolated cooling, rated up to 3500  $V_{RMS}$
- ✓ Easy mounting to heat sink
- ✓ Heat sink grounded.

## Voltage

Parameter	Symbol	Rating	Units
Maximum Repetitive Off-State Voltage <small>Notes: 1, 3, 4, 5, 6, 7</small>	$V_{DRM}$	1200 ~ 1800	Volts
Maximum Repetitive Reverse Voltage <small>Notes: 1, 3, 4, 5, 6</small>	$V_{RRM}$	1200 ~ 1800	Volts
Maximum non repetitive Surge of Reverse Voltage <small>Notes: 2, 3, 4, 5, 6</small>	$V_{RSM}$	$V_{RRM} + 100$	Volts
Critical rate of rising off-state Voltage, Linear to 80% of $V_{DRM}$ <small>Note: 2</small>	$dv/dt$	500	$V/\mu s$
<small>Note 1: <math>T_j</math> 25°C. Note 2: <math>T_j</math> 125°C. Note 3: Measured at the peak of the sine wave, Note 4: Below 0°C derate <math>V_{DRM}</math> and <math>V_{RRM}</math> 10%.                      Note 5: <math>V_{DRM}</math> and <math>V_{RRM}</math> have <math>I_{DRM}</math>, <math>I_{RRM}</math> of up to 20mA. Note 6: <math>V_{DR}</math> and <math>V_{RR}</math> have typical <math>I_{DR}</math>, <math>I_{RR}</math> of 2-3mA. Note 7: For DC applications derate <math>V_{DRM}</math> 45%.</small>			
Specifying voltage:			
1200V, PSMT25N12	1400V, PSMT25N14	1600V, PSMT25N16	1800V, PSMT25N18
Above 1800V inquire about availability.			

## Gate

Parameter	Symbol	Rating			Units
		Temp.	Typ.	Max.	
Gate Trigger Voltage <small>Note 3</small>	$V_{GT}$	-20°C	0.9	2	Volts
		25°C	0.8		
		125°C	1		
Maximum Gate Trigger Current <small>Notes 1,3</small>	$I_{GT}$	50 ~ 120			mA
Minimum Forward Current to Latch on-state <small>Notes 1, 5</small>	$I_L$	400			mA
Maximum permissible Gate Voltage not to Trigger <small>Notes 1,3</small>	$V_{GDM}$	250			mV
Maximum permissible Gate Current not to Trigger <small>Notes 1, 3</small>	$I_{GDM}$	5			mA
Maximum peak non repetitive Gate Voltage <small>Notes 2, 3</small>	$V_{GM}$	5			Volts
Maximum Negative Gate Voltage <small>Notes 2, 4</small>	$-V_{GM}$	4			Volts
Maximum non repetitive Gate Current <small>Notes 2, 3</small>	$I_{GM}$	1.5			Amperes
Maximum Repetitive Gate Current <small>Notes 2, 3</small>	$I_{GRM}$	800			mA
Average Gate Power (recommended) <small>Note 2, 3</small>	$P_{G(AVE)}$	50 ~ 250			mW
<small>Note 1: <math>T_j</math> 25°C. Note 2: <math>T_j</math> 125°C. Note 3: Rectangular pulse, <math>t_b \leq 8.3</math> ms. Note 4: Rectangular <math>-V_{DC}</math> pulse, <math>t_b \leq 8.3</math> ms. Note 5: Test conditions: <math>I_{DC}</math> <math>R_{\theta} = 12\Omega</math>.</small>					

## Amperage

Parameter	Symbol	Rating	Units
Maximum, Average, On state, Current <small>Notes: 1, 2</small>	$I_{T(AVE)}$	25	Amperes
Maximum, RMS, On state, Current <small>Notes: 1, 3</small>	$I_{T(RMS)}$	39	Amperes
Maximum non repetitive, Surge, On state, Current, with no reverse voltage reapplied.	$I_{TSM} 0\%V_{RRM}$	1.7	kA
Maximum non repetitive, Surge, On state, Current, with maximum reverse voltage reapplied. <small>Notes: 2, 4</small>	$I_{TSM} 100\%V_{RRM}$	1.4	kA
Critical rate of rising On-state Current, non repetitive <small>Note: 6, 7</small>	$di/dt$	150	$A/\mu s$
Holding Current <small>Notes: 1, 5</small>	$I_H$	250	mA
Maximum On State Voltage drop at Maximum On State Current	$V_{TM} @ I_{TM}$	1.6 @ 80	V @ A
$I_{DRM}$ = Maximum (threshold), Repetitive, Off-State, Current. <small>Note: 1</small> $I_{RRM}$ = Maximum (threshold), Repetitive, Reverse, Current. <small>Note: 1</small>	$I_{DRM}$ & $I_{RRM}$	20	mA
Fuse's absolute maximum $I^2 t$ with no reverse voltage	$I^2 t, 0\% V_{RR}$	730	Amperes
Fuse's absolute maximum $I^2 t$ with up to 100% of $V_{RRM}$	$I^2 t, \leq 100\% V_{RRM}$	510	Amperes
<small>Note 1: <math>T_j</math> 55°C, Air Cooled Note 2: 120° Conduction, 60 Hz, Sinewave Note 3: 180° Conduction, 60 Hz, Sinewave                      Note 4: Test conditions <math>I_{DC}</math> <math>R_{\theta} = 12\Omega</math> Note 5: Switching from <math>V_{DRM} &lt; 1000V</math> Note 6: In addition to 0.2<math>\mu F</math> and 20<math>\Omega</math> snubber circuit</small>			

Release date: 2010-10-11