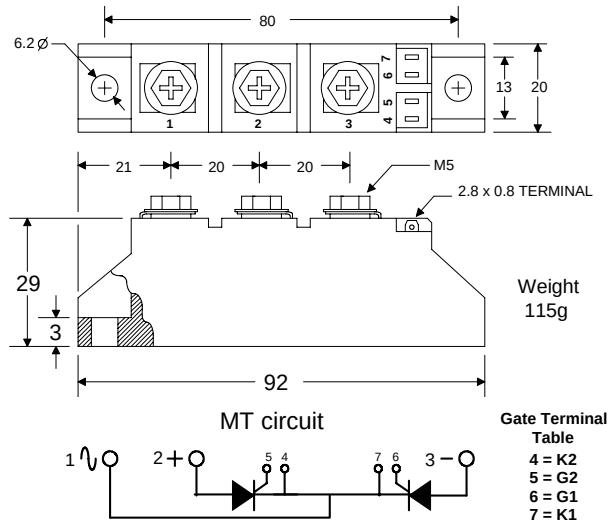
TO-240AA compatible package



MT circuit

Gate Terminal Table
4 = K2
5 = G2
6 = G1
7 = K1

Part number scheme

PS	**MT**	**91**	**N**	**16**	**KNX**
1	2	3	4	5	6

1) Power Semiconductors initials
2) Circuit designation
3) Series number
4) Designates standard recovery time
5) Voltage Multiplier (example: 16 x 100 = 1600 Volts)
6) Proprietary suffix

Features:

- ✓ All diffused silicone junctions.
- ✓ Standard recovery time for phase control applications.
- ✓ Module package compatible with JEDEC T0-240AA.
- ✓ Thick copper base plate.
- ✓ Isolated cooling, rated up to 3500 V_{RMS}
- ✓ Easy mounting to heat sink
- ✓ Heat sink grounded.

Voltage

Parameter	Symbol	Rating	Units
Maximum Repetitive Off-State Voltage Notes: 1, 3, 4, 5, 6, 7	V_{DRM}	1200 ~ 1800	Volts
Maximum Repetitive Reverse Voltage Notes: 1, 3, 4, 5, 6	V_{RRM}	1200 ~ 1800	Volts
Maximum non repetitive Surge of Reverse Voltage Notes: 2, 3, 4, 5, 6	V_{RSM}	V_{RRM} + 100	Volts
Critical rate of rising off-state Voltage, Linear to 80% of V_{DRM} Note: 2	dv/dt	500	V/μs
Note 1: T_J 25ºC. Note 2: T_J 125ºC. Note 3: Measured at the peak of the sine wave, Note 4: Below 0ºC derate V_{DRM} and V_{RRM} 10%.			
Note 5: V_{DRM} and V_{RRM} have I_{DRM}, I_{RRM} of up to 20mA. Note 6: V_{DR} and V_{RR} have typical I_{DR}, I_{RR} of 2~3mA. Note 7: For DC applications derate V_{DRM} 45%.			
Specifying voltage: 1400V, PSMT91N14 1800V, PSMT91N18			
1200V, PSMT91N12 1600V, PSMT91N16 Above 1800V inquire about availability.			

Gate

Parameter	Symbol	Rating			Units
		Temp.	Typ.	Max.	
Gate Trigger Voltage Note 3	V_{GT}	-20º C	0.9	2	Volts
		25º C	0.8		
		125º C	1		
Maximum Gate Trigger Current Notes 1,3	I_{GT}	50 ~ 120			mA
Minimum Forward Current to Latch on-state Notes 1, 5	I_L	400			mA
Maximum permissible Gate Voltage not to Trigger Notes 1,3	V_{GDM}	250			mV
Maximum permissible Gate Current not to Trigger Notes 1, 3	I_{GDM}	5			mA
Maximum peak non repetitive Gate Voltage Notes 2, 3	V_{GM}	5			Volts
Maximum Negative Gate Voltage Notes 2, 4	$-V_{GM}$	4			Volts
Maximum non repetitive Gate Current Notes 2, 3	I_{GM}	1.5			Amperes
Maximum Repetitive Gate Current Notes 2, 3	I_{GRM}	800			mA
Average Gate Power (recommended) Note 2, 3	$P_{G(AVE)}$	50 ~ 250			mW
Note 1: T_J 25ºC. Note 2: T_J 125ºC. Note 3: Rectangular pulse, $t_p \leq 8.3$ ms. Note 4: Rectangular $-V_{DC}$ pulse, $t_p \leq 8.3$ ms. Note 5: Test conditions: I_{DC} $R_L = 12\Omega$.					

Current

Parameter	Symbol	Rating	Units
Maximum, Average, On state, Current, Notes: 1, 2	$I_{T(AVE)}$	90	Amperes
Maximum, RMS, On state, Current Notes: 1, 3	$I_{T(RMS)}$	145	Amperes
Maximum non repetitive, Surge. On state, Current ,with no reverse voltage reapplied.	I_{TSM} 0%V_{RRM}	1.7	kA
Maximum non repetitive, Surge, On state, Current, with maximum reverse voltage reapplied. Notes: 2, 4	I_{TSM} 100%V_{RRM}	1.4	kA
Critical rate of rising On-state Current, non repetitive Note: 6, 7	di/dt	150	A/μs
Holding Current Notes: 1, 5	I_H	250	mA
Maximum On State Voltage drop at Maximum On State Current	V_{TM} @ I_{TM}	1.4 @ 200	V @ A
I_{DRM} = Maximum (threshold), Repetitive, Off-State, Current. Note: 1 I_{RRM} = Maximum (threshold), Repetitive, Reverse, Current. Note: 1	I_{DRM} & I_{RRM}	20	mA
Fuse's absolute maximum I^2t with no reverse voltage	I^2 t, 0% V_{RR}	14.8	kA
Fuse's absolute maximum I^2t with up to 100% of V_{RRM}	I^2 t, ≤ 100% V_{RRM}	9.69	kA
Note 1: T_J 55ºC, Air Cooled Note 2: 120º Conduction, 60 Hz, Sinewave Note 3: 180º Conduction, 60 Hz, Sinewave			
Note 4: Test conditions I_{DC} $R_L = 12\Omega$ Note 5: Switching from $V_{DRM} \leq 1000V$ Note 6: In addition to 0.2μF and 20Ω snubber circuit			